

## WHAT IS CLAIMED IS:

1           1. Control circuitry for adjusting a power supply level,  
2 VDD, of a digital processing component having varying operating  
3 frequencies, said control circuitry comprising:

4           N delay cells coupled in series, each of said N delay  
5 cells having a delay D determined by a value of VDD, such that a  
6 clock edge applied to an input of a first delay cell ripples  
7 sequentially through said N delay cells; and

8           power supply adjustment circuitry capable of adjusting  
9 VDD, said power supply adjustment circuitry operable to (i)  
10 monitor outputs of at least a K delay cell and a K+1 delay cell,  
11 (ii) determine that said clock edge has reached an output of said  
12 K delay cell and has not reached an output of said K+1 delay  
13 cell, and (iii) generate a control signal capable of adjusting  
14 VDD.

1           2. The control circuitry for adjusting a power supply  
2 level as set forth in Claim 1 wherein said power supply  
3 adjustment circuitry determines that said clock edge has reached  
4 said K delay cell output and has not reached said K+1 delay cell  
5 output when a next sequential clock edge is applied to said first  
6 delay cell input.

1           3.    The control circuitry for adjusting a power supply  
2    level as set forth in Claim 2 wherein a total delay from said  
3    first delay cell input to said K delay cell output is greater  
4    than a maximum delay of said digital processing component scaled  
5    by a constant factor.

1           4.    The control circuitry for adjusting a power supply  
2    level as set forth in Claim 2 wherein said power supply  
3    adjustment circuitry increases VDD if said clock edge has not  
4    reached said K delay cell output.

1           5.    The control circuitry for adjusting a power supply  
2    level as set forth in Claim 2 wherein said power supply  
3    adjustment circuitry decreases VDD if said clock edge has reached  
4    said K+1 delay cell output.

1           6.    The control circuitry for adjusting a power supply  
2    level as set forth in Claim 2 wherein said power supply  
3    adjustment circuitry is further operable to monitor outputs of at  
4    least a K-1 delay cell, said K delay cell, said K+1 delay cell,  
5    and a K+2 delay cell.

1           7. The control circuitry for adjusting a power supply  
2 level as set forth in Claim 6 wherein said power supply  
3 adjustment circuitry is further operable to determine that said  
4 clock edge has reached an output of said K-1 delay cell and said  
5 K delay cell output and has not reached said K+1 delay cell  
6 output.

1           8. The control circuitry for adjusting a power supply  
2 level as set forth in Claim 7 wherein said power supply  
3 adjustment circuitry increases VDD in relatively large  
4 incremental steps if said clock edge has not reached said K-  
5 1 delay cell output.

1           9. The control circuitry for adjusting a power supply  
2 level as set forth in Claim 8 wherein said power supply  
3 adjustment circuitry increases VDD in relatively small  
4 incremental steps if said clock edge has reached said K-1 delay  
5 cell output but has not reached said K delay cell output.

1           10. The control circuitry for adjusting a power supply  
2 level as set forth in Claim 7 wherein said power supply  
3 adjustment circuitry decreases VDD in relatively large  
4 incremental steps if said clock edge has reached said K+1 delay  
5 cell output and said K+2 delay cell output.

1           11. The control circuitry for adjusting a power supply  
2 level as set forth in Claim 10 wherein said power supply  
3 adjustment circuitry decreases VDD in relatively small  
4 incremental steps if said clock edge has reached said K+1 delay  
5 cell output but has not reached said K+2 delay cell output.

1           12. A method of operating control circuitry for adjusting a  
2 power supply level, VDD, of a digital processing component having  
3 varying operating frequencies, said method of operating said  
4 control circuitry comprising the steps of:

5           applying a clock edge to an input of a first one of N  
6 delay cells coupled in series, each of said N delay cells having  
7 a delay D determined by a value of VDD, said applied clock edge  
8 rippling sequentially through said N delay cells;

9           monitoring outputs of at least a K delay cell and a K+1  
10 delay cell;

11           determining that said clock edge has reached an output  
12 of said K delay cell and has not reached an output of said K+1  
13 delay cell; and

14           generating a control signal capable of adjusting VDD.

1           13. The method of operating control circuitry for adjusting  
2 a power supply level, VDD, as set forth in Claim 12 further  
3 comprising the step of determining that said clock edge has  
4 reached said K delay cell output and has not reached said K+1  
5 delay cell output when a next sequential clock edge is applied to  
6 said first delay cell input.

1           14. The method of operating control circuitry for adjusting  
2 a power supply level, VDD, as set forth in Claim 13 wherein a  
3 total delay from said first delay cell input to said K delay cell  
4 output is greater than a maximum delay of said digital processing  
5 component scaled by a constant factor.

1           15. The method of operating control circuitry for adjusting  
2 a power supply level, VDD, as set forth in Claim 13 further  
3 comprising the step of increasing VDD if said clock edge has not  
4 reached said K delay cell output.

1           16. The method of operating control circuitry for adjusting  
2 a power supply level, VDD, as set forth in Claim 13 further  
3 comprising the step of decreasing VDD if said clock edge has  
4 reached said K+1 delay cell output.

1           17. The method of operating control circuitry for adjusting  
2 a power supply level, VDD, as set forth in Claim 13 further  
3 comprising the step of monitoring outputs of at least a K-1 delay  
4 cell, said K delay cell, said K+1 delay cell, and a K+2 delay  
5 cell.

1           18. The method of operating control circuitry for adjusting  
2 a power supply level, VDD, as set forth in Claim 17 further  
3 comprising the step of determining that said clock edge has  
4 reached an output of said K-1 delay cell and said K delay cell  
5 output and has not reached said K+1 delay cell output.

1           19. The method of operating control circuitry for adjusting  
2 a power supply level, VDD, as set forth in Claim 18 further  
3 comprising the step of increasing VDD in relatively large  
4 incremental steps if said clock edge has not reached said K-  
5 1 delay cell output.

1           20. The method of operating control circuitry for adjusting  
2 a power supply level, VDD, as set forth in Claim 19 further  
3 comprising the step of increasing VDD in relatively small  
4 incremental steps if said clock edge has reached said K-1 delay  
5 cell output but has not reached said K delay cell output.

1           21. The method of operating control circuitry for adjusting  
2 a power supply level, VDD, as set forth in Claim 18 further  
3 comprising the step of decreasing VDD in relatively large  
4 incremental steps if said clock edge has reached said K+1 delay  
5 cell output and said K+2 delay cell output.

1           22. The method of operating control circuitry for adjusting  
2 a power supply level, VDD, as set forth in Claim 21 further  
3 comprising the step of decreasing VDD in relatively small  
4 incremental steps if said clock edge has reached said K+1 delay  
5 cell output but has not reached said K+2 delay cell output.



23. A digital circuit comprising:

- a digital processing component capable of operating at different clock frequencies;
- an adjustable clock source capable of supplying variable clock frequencies to said digital processing component;
- an adjustable power supply capable of supplying a variable power supply level, VDD, to said digital processing component; and
- control circuitry for adjusting VDD comprising:
  - N delay cells coupled in series, each of said N delay cells having a delay D determined by a value of VDD, such that a clock edge applied to an input of a first delay cell ripples sequentially through said N delay cells; and
  - power supply adjustment circuitry capable of adjusting VDD, said power supply adjustment circuitry operable to (i) monitor outputs of at least a K delay cell and a K+1 delay cell, (ii) determine that said clock edge has reached an output of said K delay cell and has not reached an output of said K+1 delay cell, and (iii) generate a control signal capable of adjusting VDD.

1           24. The digital circuit as set forth in Claim 23 wherein  
2 said power supply adjustment circuitry determines that said clock  
3 edge has reached said K delay cell output and has not reached  
4 said K+1 delay cell output when a next sequential clock edge is  
5 applied to said first delay cell input.

1           25. The digital circuit as set forth in Claim 24 wherein a  
2 total delay from said first delay cell input to said K delay cell  
3 output is greater than a maximum delay of said digital processing  
4 component.

1           26. The digital circuit as set forth in Claim 24 wherein  
2 said power supply adjustment circuitry increases VDD if said  
3 clock edge has not reached said K delay cell output.

1           27. The digital circuit as set forth in Claim 24 wherein  
2 said power supply adjustment circuitry decreases VDD if said  
3 clock edge has reached said K+1 delay cell output.

1           28. The digital circuit as set forth in Claim 24 wherein  
2 said power supply adjustment circuitry is further operable to  
3 monitor outputs of at least a K-1 delay cell, said K delay cell,  
4 said K+1 delay cell, and a K+2 delay cell.

1           29. The digital circuit as set forth in Claim 28 wherein  
2 said power supply adjustment circuitry is further operable to  
3 determine that said clock edge has reached an output of said K-  
4 1 delay cell and said K delay cell output and has not reached  
5 said K+1 delay cell output.

1           30. The digital circuit as set forth in Claim 29 wherein  
2 said power supply adjustment circuitry increases VDD in  
3 relatively large incremental steps if said clock edge has not  
4 reached said K-1 delay cell output.

1           31. The digital circuit as set forth in Claim 30 wherein  
2 said power supply adjustment circuitry increases VDD in  
3 relatively small incremental steps if said clock edge has reached  
4 said K-1 delay cell output but has not reached said K delay cell  
5 output.

1           32. The digital circuit as set forth in Claim 29 wherein  
2 said power supply adjustment circuitry decreases VDD in  
3 relatively large incremental steps if said clock edge has reached  
4 said K+1 delay cell output and said K+2 delay cell output.

1           33. The digital circuit as set forth in Claim 32 wherein  
2 said power supply adjustment circuitry decreases VDD in  
3 relatively small incremental steps if said clock edge has reached  
4 said K+1 delay cell output but has not reached said K+2 delay  
5 cell output.